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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/657,898	09/09/2003	Thomas Steinecke	WMP-IFT-964	5647

24131 7590 07/25/2005

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EXAMINER	
CAO, PHAT X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

Office Action Summary	Application No.	Applicant(s)	
	10/657,898	STEINECKE ET AL.	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *18 and 19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-13,16 and 17* is/are rejected.

7)☒ Claim(s) *4,5,14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3 and 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori (US. 5,949,098) in view of Yonesaka (US. 6,696,712).

Regarding claims 1 and 6, Mori (Fig. 3) discloses an electronic device, comprising: a semiconductor chip (column 2, lines 7-9); the semiconductor chip having a plurality of metallization layers 370/350/330/310 and a plurality of insulation layers 360/340/320 configured alternately one above another on the active top side; the plurality of metallization layers including topmost metallization layers having a plurality of voltage supply structures 310/330/350 (column 4, lines 39-53) and lower metallization layers disposed underneath the topmost metallization layers and having a plurality of signal line structures 371/372/373 (column 5, lines 1-6); the plurality of insulation layers 360/340/320 formed with a plurality of passage contacts 321/341/361 connecting the plurality of voltage supply structures or the plurality of signal line structures to the contact areas; the topmost metallization layers 350/330/310 having ones of the plurality of passage contacts 321/341/361 connected to the contact areas; the topmost metallization layers 350/330/310 having at least a first one of the plurality of voltage supply structures 332 for a ground or low supply potential and a second one of the

plurality of voltage supply structures 331 for a power or high supply potential (column 5, lines 40-49); the first one of the plurality of voltage supply structures 332 being insulated from the second one of the plurality of voltage supply structures 331; the first one of the plurality of voltage supply structures 332 of the topmost metallization layers 350/330/310 having a grid of supply interconnect 332 configured parallel to one another (see interconnects 332 in metallization layer 330), the second one of the plurality of voltage supply structures 331 of the topmost metallization layers 350/330/310 having a grid of supply interconnects 331 configured parallel to one another (see interconnects 331 arranged in metallization layer 330); and the grid of supply interconnects 332 of the first one of the plurality of voltage supply structures being rotated parallel relative to the grid of supply interconnects 331 of the second one of the plurality of voltage supply structures; wherein the supply interconnects 332 of the grid of the first one of the plurality of voltage structures 332 all have a ground supply potential that is different from the power supply potential of the supply interconnects 331 of the grid of the second one of the plurality of voltage supply structures 331.

Mori does not disclose that the semiconductor chip having active topside with a plurality of contact areas.

However, Yonesaka (Fig. 2) teaches the forming of a semiconductor chip having active topside with a plurality of contact areas 3a-3e, and the forming of the plurality of insulation layers formed with a plurality of passage contacts connecting the plurality of metallization layers to the plurality of contact areas 3a-3e of the active topside. Accordingly, it would have been obvious to provide o an active top side of the

semiconductor chip of Mori with a plurality of contact areas in order to provide the electrical contacts of the voltage supply lines/signal lines to the circuits formed in the substrate of the semiconductor chip, as taught by Yonesaka (see Fig. 2 and column 5, lines 56-63).

Regarding claim 2, Mori further discloses that the semiconductor chip includes an integrated circuit subdivided into a plurality of functional module regions 421 and 422 (see Fig. 4), and each one of the plurality of module regions 421 and 422 has a plurality of passage contacts connecting one of the plurality of contact areas to the first one of the plurality of voltage supply structures 332 and to the second one of the plurality of voltage supply structures 331 (see Fig. 3).

Regarding claim 3, as discussed in details above, the combination of Mori and Yonesaka substantially reads on the interconnect structures and the electrical connections as claimed. Yonesaka (Fig. 2) further teaches that the semiconductor chip having an integrated circuit formed near the active topside of the semiconductor substrate 1. The combination of Mori and Yonesaka does not teach that the electrical connections are wired using place-route programs.

However, it would have been obvious to use place-route programs for wiring the electrical connections because this wiring technology is well known and commonly use for providing the arrangement of the electrical connections in each of the metallization planes of the integrated circuit (see "Background" of Applicant's invention, page 2)..

Regarding claim 7, Mori (Fig. 3) further discloses that ones of the plurality of insulation layers located between the topmost metallization layers 350/330/310 have a

thickness dimensioned to provide an electrical capacitance c31/c32/c33 that is as high as possible with sufficient dielectric strength at areas of the topmost metallization layers that are configured one above another (column 5, lines 40-49).

Regarding claims 8-9, it would have been obvious to form the plurality of metallization layers and the insulation layers of Mori with the materials as claimed because such metallization materials (i.e., aluminum, copper) and insulation materials (i.e., silicon dioxide, silicon nitride) are well known and commonly used for providing the electrical interconnections and insulations in the interconnect structures.

Regarding claim 10, Mori (Fig. 6) further discloses that the supply interconnects of the grid of the first one of the plurality of voltage supply structures 613/614 have a thickness and a width that are greater than the thickness and the width of the interconnects of the plurality of signal line structures 651/652, and the supply interconnects of the grid of the second one of the plurality of voltage supply structures 611/612 have a thickness and the width that are greater than the thickness and the width of the interconnects of the plurality of signal line structures 651/652.

3. Claims 11-13 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori (US. 5,949,098) in view of Yonesaka (US. 6,696,712) and Chua et al (US. 6,825,553).

Regarding claims 11 and 16, as discussed in details above (see ground of rejection of claims 1 and 6 above), the combination of Mori and Yonesaka substantially reads on the above claims, including the forming of a plurality of module regions 421 and 422 configured below the topmost metallization layers (see Mori, Figs. 3-4).

Neither Mori nor Yonesaka disclose a semiconductor wafer having a plurality of semiconductor chip positions configured in rows and columns.

However, Chua (Fig. 4) teaches the forming of a semiconductor wafer having semiconductor chip positions 406 configured in rows and columns. Accordingly, it would have been obvious to form a plurality of semiconductor chip positions of Mori configured in rows and columns on a semiconductor wafer because the forming of chips on the wafer is well known and commonly used in the semiconductor wafer technology for forming a plurality of semiconductor chips at a same time, as taught by Chua (column 8, lines 44-60).

Regarding claim 12, , Mori further discloses that the semiconductor chip includes an integrated circuit subdivided into a plurality of functional module regions 421 and 422 (see Fig. 4), and each one of the plurality of module regions 421 and 422 has a plurality of passage contacts connecting one of the plurality of contact areas to the first one of the plurality of voltage supply structures 332 and to the second one of the plurality of voltage supply structures 331 (see Fig. 3).

Regarding claim 13, as discussed in details above, the combination of Mori and Yonesaka substantially reads on the interconnect structures and the electrical connections as claimed. Yonesaka (Fig. 2) further teaches that the semiconductor chip having an integrated circuit formed near the active topside of the semiconductor substrate 1. The combination of Mori and Yonesaka does not teach that the electrical connections are wired using place-route programs.

However, it would have been obvious to use place-route programs for wiring the electrical connections because this wiring technology is well known and commonly use for providing the arrangement of the electrical connections in each of the metallization planes of the integrated circuit (see "Background" of Applicant's invention, page 2)..

Regarding claim 17, Mori (Fig. 3) further discloses that ones of the plurality of insulation layers located between the topmost metallization layers 350/330/310 have a thickness dimensioned to provide an electrical capacitance c31/c32/c33 that is as high as possible with sufficient dielectric strength at areas of the topmost metallization layers that are configured one above another (column 5, lines 40-49).

Allowable Subject Matter

4. Claims 4-5 and 14-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose the supply interconnects of the grid of the first one of the plurality of voltage supply structures and the second one of the plurality of voltage supply structures each alternatively having different electrical supply potentials.

Response to Arguments

5. Applicant argues that Mori does not suggest the grid of supply interconnects of the first one of the plurality of voltage supply structures being rotated orthogonally relative to the grid of supply interconnects of the second one of the plurality of voltage supply structures.

This argument is not persuasive because the feature of having the grid of supply interconnects of the first one of the plurality of voltage supply structures being rotated orthogonally relative to the grid of supply interconnects of the second one of the plurality of voltage supply structures does not seem to be required by the claim language. Therefore, in contrary to Applicant's assertions, Mori does suggest the invention as claimed because Fig. 30 of Mori clearly discloses the grid of supply interconnects 332 of the first one of the plurality of voltage supply structures being rotated parallel relative to the grid of supply interconnects 331 of the second one of the plurality of voltage supply structures.

Applicant argues that the feature of having the grid of supply interconnects 332 being rotated parallel relative to the grid of supply interconnects 331 as suggested by Mori does not suggest the invention as claimed because the phrase "being rotated parallel" is not recited in the claim language.

It is noted that claims in a pending application should be given their broadest reasonable interpretation. In re Pearson, 494 F.2d 1399, 181 USPQ641 (CCPA 1974). In this case, the claim language does not specifically recite how the grid of one supply interconnects "being rotated" relative to the grid of other supply interconnects. Therefore, the phrase "being rotated" can be interpreted as "being rotated" in any direction. Thus, Mori does suggest the invention as claimed because Mori's Fig. 3 discloses the grid of supply interconnects 332 "being rotated" or oriented parallel relative to the grid of supply interconnects 331.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is 571-272-1703. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
July 22, 2005

PHAT X. CAO
PRIMARY EXAMINER